# PATENT ABSTRACTS OF JAPAN

(11)Publication number : **08-306820**
(43)Date of publication of application : **22.11.1996**

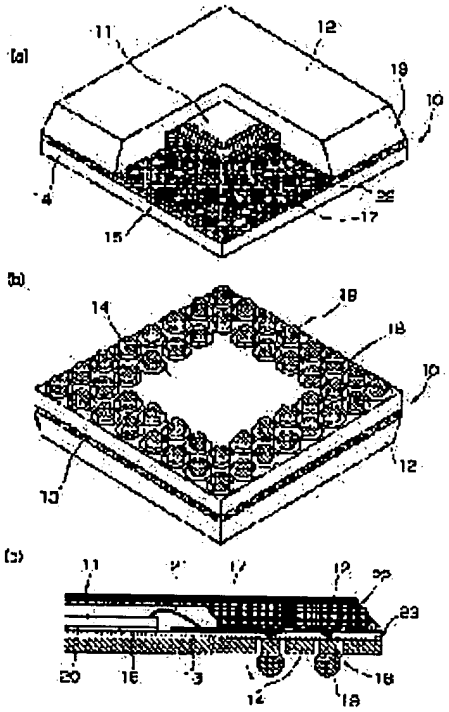
(51)Int.Cl. **H01L 23/12**

(21)Application number : **07-127395**
(22)Date of filing : **28.04.1995**

(71)Applicant : **NEC CORP**
(72)Inventor : **SUZUKI KATSUNOBU**
**SUZUKI KATSUHIKO**
**HAGA AKIRA**
**TANMACHI ISAMU**
**UCHIDA HIROYUKI**

## (54) SEMICONDUCTOR DEVICE, PACKAGE FOR SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:
PURPOSE: To manufacture a semiconductor device excellent in humidity resistance, reliability and electric performance.
CONSTITUTION: A polyimide layer 13 and copper foil patterns 15, 17 are formed on plate type metal bases 14, 18, and a lamination structure body is constituted. The metal bases are constituted of a ground pattern 14 maintained at the earth potential and many land patterns 18 where solder balls 19 for mounting are formed. The copper foil patterns consist of an island pattern 15 where an LSI 11 is mounted and inner wiring 17 connected with the electrodes of the LSI chip 11. The metal base patterns 14, 18 are electrically connected with the internal wiring 17 via through-holes 22 formed by electroplating. A cap 12 covers the LSI 11 and the wiring pattern 17, and is bonded to the lamination structure body, thereby hermetically maintaining the internal space. A semiconductor device excellent in electric reliability and performance can be manufactured.



LEGAL STATUS

| | |
|---|---|
| [Date of request for examination] | 28.04.1995 |
| [Date of sending the examiner's decision of rejection] | |
| [Kind of final disposal of application other than the examiner's decision of rejection or application converted registration] | |
| [Date of final disposal for application] | |
| [Patent number] | 2679681 |
| [Date of registration] | 01.08.1997 |
| [Number of appeal against examiner's decision of rejection] | |
| [Date of requesting appeal against examiner's decision of rejection] | |
| [Date of extinction of right] | |

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CLAIMS

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[Claim(s)]
[Claim 1] The package for semiconductor devices characterized by this grand pattern and a land pattern, and the aforementioned circuit pattern flowing through the aforementioned insulating layer through the through hole penetrated in a predetermined position including the grand pattern and two or more land patterns which are characterized by providing the following, and with which it was constituted as a laminated-structure object, and the aforementioned metal base pattern was insulated mutually electrically. The metal base pattern which consists of the metal plate which makes copper or aluminum a principal component, and has a predetermined pattern configuration. The insulating layer which consists of the organic system insulator formed on this metal base pattern at least. The thin film pattern which consists of the metallic foil which has the predetermined pattern configuration including a circuit pattern formed on this insulating layer.
[Claim 2] The package for semiconductor devices according to claim 1 in which a bump is formed on the aforementioned circuit pattern.
[Claim 3] The package for semiconductor devices according to claim 1 whose aforementioned thin film pattern has an island pattern for carrying a semiconductor chip.
[Claim 4] The package for semiconductor devices according to claim 1 constituted as a cavity to which the aforementioned thin film pattern and an insulating layer are removed, and the position in which a semiconductor chip is carried exposes the aforementioned metal base pattern.
[Claim 5] The claim 1 which some aforementioned grand patterns [ at least ] consist of as a ring pattern arranged in the shape of a frame at the periphery section of the aforementioned laminated-structure object, or the package for semiconductor devices given in any 1 of 4.
[Claim 6] The claim 1 from which the aforementioned metal base pattern consists of a ring pattern arranged in the shape of a frame at the periphery section of the aforementioned laminated-structure object, a central pattern which had the circumference surrounded by this ring pattern, and two or more aforementioned land patterns, and either [ at least ] the aforementioned ring pattern or a central pattern constitutes the aforementioned grand pattern, or the package for semiconductor devices given in any 1 of 4.
[Claim 7] The package for semiconductor devices according to claim 6 by which a chip is arranged between the aforementioned ring pattern and the aforementioned central pattern.
[Claim 8] The claim 1 further equipped with the insulating resin layer which coats the front face of the aforementioned metal base patterns other than the aforementioned land pattern, and the crevice portion of this metal base pattern, or the package for semiconductor devices given in any 1 of 7.
[Claim 9] The claim 1 through which is equipped with the combination of 1 more or more sets of another insulating layers, and a thin film pattern on the aforementioned thin film pattern, and the thin film pattern which counters mutually flows through the through hole formed in the predetermined position of the insulating layer which intervenes between [ this ] thin film patterns, or the package for semiconductor devices given in any 1 of 8.
[Claim 10] The package for semiconductor devices containing the ring closure pattern with which the aforementioned thin film pattern of the best layer is arranged in the shape of a frame at the periphery section of a laminated-structure object according to claim 9.
[Claim 11] The claim 1 in which the aforementioned thin film pattern contains the ring closure pattern arranged in the shape of a frame at the periphery section of the aforementioned laminated-structure object, or the package for semiconductor devices given in any 1 of 8.
[Claim 12] The claim 1 which the aforementioned thin film pattern and an insulating layer are removed in the shape of a frame in the periphery section of the aforementioned laminated-structure object, and a metal base pattern is exposed in the this removed periphery section, and constitutes the ring closure section, or the package for semiconductor devices given in any 1 of 8.
[Claim 13] The claim 1 in which the aforementioned through hole is formed of plating, or the package for semiconductor devices given in any 1 of 12.
[Claim 14] The package for semiconductor devices characterized by having joined the laminated-structure object of both this mutually through the middle insulating layer so that it might have a claim 1 or two laminated-structure objects given in any 1 of 9 and the aforementioned thin film pattern might face each other, and for the thin film pattern of the laminated-structure

object of both this having flowed through the through hole formed in the predetermined position in a middle insulating layer, and the metal base pattern of one laminated-structure object containing a flip chip bump.
[Claim 15] The semiconductor device characterized by being attached in the aforementioned laminated-structure object with the bonding which is equipped with the semiconductor chip carried in a claim 1 and a claim 3, or the package for semiconductor devices and this package given in any 1 of 13, and this semiconductor chip depends for any of an organic system resin, a metal mixing resin, or a low melting point metal being.
[Claim 16] The semiconductor device characterized by having the semiconductor chip carried in the package for semiconductor devices and this package according to claim 2, and carrying out flip chip bonding of this semiconductor chip through a resin or a low melting point metal on the aforementioned bump.
[Claim 17] The semiconductor device according to claim 15 or 16 further equipped with the cap of the metal which closes airtightly the thin film pattern side of the aforementioned laminated-structure object, or the product made of an organic resin.
[Claim 18] The claim 15 which each of the aforementioned land pattern equips with a solder ball, or a semiconductor device given in any 1 of 17.
[Claim 19] The claim 15 which equips the lower part of the aforementioned semiconductor chip with the thermolysis through hole which penetrates the aforementioned grand pattern at least and by which the thermolysis solder ball was formed in the position which adjoins the thermolysis through hole of this grand pattern, or a semiconductor device given in any 1 of 18.
[Claim 20] The manufacture method of the package for semiconductor devices which is the method of manufacturing the package for semiconductor devices according to claim 14, and is characterized by performing the aforementioned junction by either adhesives, thermocompression bonding or the adhesion using the chemical reaction.
[Claim 21] The 2nd opening is formed in the process which forms the thin film pattern characterized by providing the following, and the position adjusted in the 1st opening of the above of the aforementioned insulating layer. A deposit is formed in 2 openings. the [ that exposes the aforementioned metal base in this 2nd opening / a process, the above 1st, and ] -- The manufacture method of the package for semiconductor devices which carries out patterning of the process which makes it flow through the aforementioned metal base and the aforementioned thin film pattern, and the aforementioned metal base, and is characterized by including the process formed in two or more patterns insulated mutually. The insulating layer which consists of an organic system insulator on the metal base which consists of the metal plate which makes copper or aluminum a principal component. Patterning of the process and the aforementioned metallic foil layer which carry out the laminating of the metallic foil layer one by one, and form a laminated-structure object is carried out, and it is the 1st opening.

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[Translation done.]

## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the structure and its manufacture method of the package for semiconductor devices using the metal substrate about the package for a semiconductor device and semiconductor devices, and its manufacture method.
[0002]
[Description of the Prior Art] In recent years, the structure of the package for semiconductor devices called BGA (BALL GRID ARRAY) is proposed. The package structure of this form is indicated by "NOV.-DEC.1992.THE FIRST VLSI PACKAGING WORKSHOP" and "March, 1994 issue NIKKEI MICRODEVICES", and efforts for utilization are advanced. Here explains the structure of the conventional BGA with reference to a drawing.
[0003] Drawing 12 is BGA (the conventional technology 1) indicated by "March, 1994 issue NIKKEI MICRODEVICES", and a substrate rear-face perspective diagram and drawing (c) of the perspective diagram and drawing (b) showing drawing (a) except for a part of surface cap are fragmentary sectional views. The external wiring 111 is formed in the internal wiring 103 and a rear face in the front face of the glass epoxy-group board 106, and the island pattern 114 for LSI loading is further formed in the front face.
[0004] The internal wiring 103 and the external wiring 111 are electrically connected by the through hole 104 in the circumference section of a package 100, and the through hole 110 for thermolysis is formed in the lower part of the island pattern 114. A land pattern is prepared in the point of the external wiring 111, and the land pattern is similarly formed directly under the thermolysis through hole 110. The portion on rear faces of a substrate other than these lands pattern is coated with the solder resist 107 which is an insulating resin. The island pattern 114 by the side of a substrate front face, a bonding wire 112, and the portion except the internal wiring 111 are also coated with a solder resist 105.
[0005] LSI101 is carried through adhesives, such as a silver paste, on the island pattern 114 of the package 100 of the above-mentioned structure, and the electrode of LSI101 and the internal wiring 103 are connected by the bonding wire 112. Furthermore, a part for the center section inside a through hole 104 is closed by the substrate front-face side with the closure resin 102 except for a part of LSI101, bonding wire 112, and internal wiring 103. After resin-seal formation, the solder balls 108 and 110 are formed on the land pattern on the rear face of a substrate. There are the solder ball 108 for electrical installation and the solder ball 109 for thermolysis only for thermolysis as solder ball.
[0006] As another conventional BGA, there is a thing (the conventional technology 2) of a "NOV.-DEC.1992.THE FIRST VLSI PACKAGINGWORKSHOP" announcement. This conventional technology is explained with reference to drawing 13 and drawing 14 . Drawing [ of drawing 13 ] (a) - (c) is the respectively same drawing as drawing 12 (a) - (c). With the structure of drawing 13 , the internal wiring 103 is formed in the front-face side of the glass epoxy-group board 106, and the external wiring 111 is formed in a rear-face side. The internal wiring 103 and the external wiring 111 are electrically connected by the through hole 104 in the predetermined position. Moreover, the land pattern which the island pattern 114 does not illustrate at the nose of cam of wiring by the side of a substrate rear face is formed in the substrate front-face side. The area which is not used for portions other than a land pattern on the back and surface bonding is coated with solder resists 107 and 105.
[0007] In the assembly of a semiconductor device, LSI101 is carried through the silver (Ag) paste 115 on an island 114, and the electrode of LSI101 and the internal wiring 103 are connected by the bonding wire 112. Furthermore, in the substrate front-face side, in a part for the center section inside a through hole 104, LSI101, the bonding wire 102, and the portion except a part of internal wiring 103 are closed by the plastic mould 113. The solder ball 108 is formed on the land pattern on the rear face of a substrate.
[0008] Drawing 14 is the structure which in addition to the structure of drawing 13 formed the thermolysis through hole 116 in the rear face of LSI101, adjoined this thermolysis through hole 116 lower part, and formed the solder ball 117 for thermolysis. The thermolysis through hole 116 and the solder ball 117 for thermolysis are connected with some land patterns.
[0009] Furthermore, there is TBGA (the conventional technology 3) indicated by "1994 March issue NIKKEI MICRODEVICES" as another conventional BGA. TBGA is the abbreviated name of TAPE-BGA and is BGA using the flexible printed circuit board (referred to also as TAB) as a substrate. Drawing 15 is the cross section showing the structure of this conventional technology 3. The predetermined printed wiring 122 is formed in both sides of the insulator polyimide

which constitutes a flexible printed circuit board 118. LSI120 is carried in both sides of a printed circuit board 118, respectively, and the TAB (tape automated bonding) lead 121 is used for connection between the electrode of each LSI120, and the internal wiring 122.
[0010] The package support plate 123 called stiffener (glass polyimide substrate) is formed in the periphery section of a package 100, and the shortage of rigidity of a flexible printed circuit board 118 is compensated, and the beer hall 119 is formed in the package support plate 123. The circuit pattern 122 on a flexible printed circuit board 118 and the solder ball 124 of a support plate 123 are connected through a beer hall 119, and the solder ball 124 is connected with the external printed circuit board which is not illustrated. Thus, electric and mechanical connection between an external printed circuit board and the package support plate 123 is made through the solder ball 124 of the package periphery section.
[0011]
[Problem(s) to be Solved by the Invention] Generally with the above-mentioned conventional BGA package structure, internal wiring and external wiring have flowed through the through hole formed with a punching drill and plating technology. However, it is difficult to fill the interior of a through hole with plating technology completely, and there is a possibility that moisture may invade from the exterior via the crevice between the formed through holes. A solder resist covers opening containing this through hole, and it is prepared in order to raise the moisture resistance of a package. However, for example compared with a hermetic-seal type package, from a solder resist, moisture invades comparatively easily and it is incorporated in a through hole or a closure resin (plastic mould). This moisture had the problem that expanding with the heat at the time of solder mounting to a printed circuit board, causing rupture of a resin layer or corroding the passivation film on the front face of LSI etc. reduced the reliability of a semiconductor device.
[0012] Moreover, the low glass epoxy resin is used for the substrate for thermal conductivity, and the heat release from an LSI rear face is small. For example, although the example which prepares two or more through holes for thermolysis is like drawing 14 for the purpose which raises thermolysis nature at an LSI rear face, the through hole for thermolysis leads to a damp-proof fall, and expansion and rupture of the resin layer by moisture, and has similarly the fault of reducing reliability.
[0013] Furthermore, in the conventional BGA, generally, since a through hole is formed by the punching drill, the path of a through hole tends to become comparatively large. therefore, in manufacturing a multi-pin package Since-izing of the wiring width of face cannot be carried out [ detailed ] using that substrate intensity falls especially, that existence of a through hole becomes the obstacle of high-density wiring, and the number of substrates increases, and printed wiring in many cases, That a design whose transmission characteristic electric in a microstrip line improves is difficult, and takes impedance matching within BGA with a bird clapper difficult for example, further In order to close by the resin, from an LSI electrode and a bonding wire being covered by the with a dielectric constants of five or more resin, especially the cross talk noise that a noise spreads between adjoining wires or by inter-electrode poses a problem, use by the high frequency band is difficult, and there are a bird clapper etc. and various problems.
[0014] On the other hand, about TBGA, there is a situation that the formation of many pins is difficult, for the structure which a solder bump can form only in the circumference of a package. Moreover, in order to take about wiring even in the periphery section of a package, there is also a problem that a wire length becomes long and causes delay of a signal.
[0015] The purpose of this invention improves and has the conventional BGA structure in view of the above, and the formation of many pins is easy for it, and it is in the structure where reliability may fully demonstrate the electric performance of LSI highly offering the new package structure which can be formed easily.
[0016]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the package for semiconductor devices concerning this invention The metal base pattern which consists of the metal plate which makes copper or aluminum a principal component, and has a predetermined pattern configuration, The insulating layer which consists of the organic system insulator formed on this metal base pattern at least, It is constituted as a laminated-structure object equipped with the thin film pattern which consists of the metallic foil which has the predetermined pattern configuration including a circuit pattern formed on this insulating layer, and which makes copper a principal component, for example. This grand pattern and a land pattern, and the aforementioned circuit pattern are characterized by flowing through the aforementioned insulating layer through the through hole penetrated in a predetermined position including the grand pattern and two or more land patterns with which the aforementioned metal base pattern was insulated mutually electrically.
[0017] Moreover, the semiconductor device concerning this invention is characterized by being attached in the aforementioned laminated-structure object with the bonding which a semiconductor chip depends for any of an organic system resin, a metal mixing resin, or a low melting point metal being, or carrying out flip chip bonding through conductive resin or a low melting point metal on a bump.
[0018] Furthermore, the manufacture method of the package for semiconductor devices of this invention The insulating layer which consists of an organic system insulator on the metal base which consists of the metal plate which makes copper or aluminum a principal component, For example, the process which carries out the laminating of the metallic foil layer which makes copper a principal component one by one, and forms a laminated-structure object, The process which forms the thin film pattern which carries out patterning of the aforementioned metallic foil layer, and contains the 1st opening, According to the process which the 2nd opening is formed [ process ] in the aforementioned insulating layer, and makes the position adjusted in the 1st opening of the above expose the aforementioned metal base in this 2nd opening, for example, electrolysis plating which uses the aforementioned metal base as an electrode the [ the above 1st and ] -- a deposit is formed in 2

openings, patterning of the process which makes it flow through the aforementioned metal base and the aforementioned thin film pattern, and the aforementioned metal base is carried out, and it is characterized by including the process formed in two or more patterns insulated mutually

[0019]

[Function] If the package for semiconductor devices of this invention is airtightly closed with caps, such as a metal or a product made of a resin, after it carries a semiconductor chip in a circuit pattern side by composition made into the laminated structure which formed the circuit pattern through the insulating layer on the metal base, a high airtight structure with the metal base and a cap will be obtained.

[0020] Moreover, since the interior of the detailed through hole formed with patterning and plating technology is filled up with plating good according to the manufacture method of the package for semiconductor devices of this invention, the invasion of moisture etc. can prevent effectively.

[0021]

[Example] Hereafter, with reference to a drawing, this invention is explained still in detail based on the suitable example of this invention. In each drawing of the package structure of each example of this invention, in order to make an understanding easy, the same reference mark is attached about the same element.

[0022] 1st example drawing 1 shows the metal BGA package structure of accomplishing the 1st example of this invention, and drawing (a) is [ a rear-face perspective diagram and drawing (c) of the front flat-tapped section notch perspective diagram and drawing (b) ] fragmentary sectional views. With the package structure of this example, the polyimide layer 13 of 0.20-0.55-micrometer ** is formed on 0.15-0.20mm front face of the Cu substrates (it is hereafter called the metal base) 14 and 18 of **, and the patterns 15 and 17 which consist of the copper foil of 0.18-0.35-micrometer ** on it further are formed. A bonding wire 21 connects with the island pattern 15 which constitutes the area in which LSI (semiconductor chip)11 is carried at the electrode of LSI11, and the pattern of copper foil consists of the internal circuit pattern 17 which takes about a substrate front-face top electrically.

[0023] The metal base on the back consists of one grand pattern 14 which supports a laminated-structure object, and many land patterns 18 for dissociating from the grand pattern 14 by patterning, and forming the solder ball 19. Each land pattern 18 has the shape of a cylindrical shape, and is formed the shape of a pillar-like notch and a concentric circle of the grand pattern 14 of the outside. The land pattern 18 is used for the wiring for the object for signals, and power supplies, and a grand pattern is maintained by grounding potential and used as grand wiring. The land pattern 18 and the grand pattern 14 can be made to match with the impedance of requests, such as 50ohms or 75 etc.ohms, by being formed as coaxial structure and performing an optimization design according to this structure.

[0024] In order to make it flow through the land pattern 18 on the rear face of a laminated circuit board and the grand pattern 14, and the internal circuit pattern 17 and the island pattern 15 on the front face of a laminated circuit board electrically, opening of the diameter of 20-30 micrometer is formed in copper foil 15 and 17 and the polyimide layer 13. A through hole 22 is embedded and formed in this opening by electrolysis plating which uses the metal bases 14 and 18 on the rear face of a substrate as an electrode, respectively. Thereby, each metal base patterns 14 and 18 and the copper foil patterns 15 and 17 are electrically connected by the corresponding through hole 22. In addition, it can replace with electrolysis plating and a through hole can also be formed by electroless deposition.

[0025] Nickel plating or gold plate is performed to the surface patterns 15 and 17, the rear-face patterns 14 and 18, and each pattern after being able to take the flow between them, and the metal BGA package 10 of this example is formed. On the occasion of LSI packaging, first, LSI11 is carried through an electroconductive glue 20 like a silver paste on the island pattern 15, and each electrode and the internal circuit pattern 17 of LSI11 are connected by the bonding wire 21. Subsequently, LSI11, a bonding wire 21, and the hollow-like cap 12 that holds a part of internal circuit pattern 17 in a building envelope are attached, and these whole is closed airtightly. Finally, the solder ball 19 is formed on each land pattern 18 of the metal base, respectively.

[0026] Generally, it will be called BGA structure and the package which forms the solder ball 19 in the shape of a grid like drawing 1 will call BGA of this invention which adopts especially the metal base metal BGA (MBGA) on these specifications. In addition, it is not limited to cap closure structure and closure structure can also adopt the mould closure by the insulating resin. When adopting mould closure, it is desirable to coat with a fluorine system resin some area of a surface island pattern and the circuit pattern used for bonding. Moreover, it is also possible to give the same coating as the portion which patterning of the metal base on the back is carried out, and does not have a base pattern. In MBGA of this example, it is also possible to form copper foil in wiring of KOPURENA structure.

[0027] 2nd example drawing 2 is drawing showing the structure of MBGA10 which constitutes the 2nd example of this invention, and drawing (a) - (c) is similarly indicated to be drawing 1 (a) - (c). Although the structure with fundamental MBGA of this example is the same as that of MBGA of the 1st example, it differs in the following points.

[0028] First, in this example, a cavity 24 is formed except for the island pattern 15 and the polyimide layer 13 of the lower part of an example 1, and it is considering as the structure of exposing the grand pattern 14 of the metal base to a front-face side in the portion of this cavity 24. Moreover, the polyimide layer 13 of a periphery portion is removed and the grand pattern of the metal base is exposed similarly. Furthermore, the coating resin layer 25 which consists of material same on the internal circuit pattern 17 and the front face of a through hole 22 the coating resin layer 27 which consists of an insulating fluorine system resin again is formed in the rear-face side front face of the grand pattern 14.

[0029] In MBGA10 of this example, LSI11 is arranged into the portion of a cavity 24. In this case, thermal conductivity arranges LSI11 to the cavity 24 interior first using resins, such as a high adhesion resin or a silver paste. Subsequently, the electrode of LSI11 and the internal wiring 17 are connected by the bonding wire 21. Then, to the grand pattern 14 of the metal base exposed in the package periphery section, similarly, thermal conductivity uses the good electroconductive glue 26, pastes up the metal cap 28, and closes LSI11, a bonding wire 21, the internal wiring 17, and through hole 16 grade in the building envelope. A semiconductor device is formed by forming the solder ball 19 on each land pattern 18 with which coating of a fluororesin finally is not carried out.

[0030] In this example, stability of the grounding potential on the rear face of LSI can be aimed at by composition using the grand pattern 14 of grounding potential like an example 1. Moreover, the thermolysis nature from an LSI rear face improves by composition whose thermal conductivity carries LSI11 in the front-face side of the grand pattern 14 through the good resin layer 20. Moreover, the metal cap 28 is maintained by grounding potential for the composition which the metal cap 28 uses conductive resin for the metal base 14, and pastes up on it directly similarly. Therefore, LSI11 is shielded by fitness from the RF noise from the outside for the structure where the circumference is surrounded by the ground potential with the cap 28 and the grand pattern 14 which were maintained, respectively.

[0031] 3rd example drawing 3 is drawing showing the structure of MBGA which constitutes the 3rd example of this invention, and (a) and (b) are a fragmentary sectional view and a rear-face perspective diagram, respectively. The structure of the copper foil in this example and a polyimide layer is the same as the 1st example, and this example differs from an example 1 in the following points. First, the metal base is constituted by the ring pattern 30 of the shape of a frame (frame) formed in the package periphery section, and the land pattern 29 of a large number arranged in the shape of a grid in the same configuration as an example 1 formed in the inside portion. The inside portion of the ring pattern 30 leaves the circular front face of each land pattern 29, and is embedded in the coating resin layer 27 of a transparent fluorine system. LSI11 is arranged on the island pattern 14 formed on the polyimide layer 13. A cap 12 pastes up with the insulating adhesives 23 on the polyimide layer 13. According to the composition of this example, since the whole package can be supported with the frame pattern 30, it is in the state which secured the intensity of a package, and its flat nature, many land patterns can be formed, and it can respond to many pin-ization easily.

[0032] 4th example drawing 4 is drawing showing the structure of MBGA which constitutes the 4th example of this invention, and (a) and (b) are drawing 3 (a) and the same drawing as (b), respectively. Although the fundamental structure of MBGA of this example is the same as the 2nd example, in the following points besides a cap 12, it differs from the 2nd example. That is, the whole metal base is divided into three portions, the ring pattern 28 of the package periphery section, the land pattern 29 of a large number arranged in the shape of a grid, and the thermolysis pattern 32 of grand combination, in this example. Coating by the solder resist 34 is given, in case it is the coating, the land pattern 29, and isomorphism-like many patterns are formed in the thermolysis pattern 32, and the metal base is exposed to the thermolysis pattern 32 in the portion. The solder ball 19 and the solder ball 33 for thermolysis are formed in each land pattern 29 front face and the pattern front face which the metal base of the thermolysis pattern 32 exposed, respectively. By composition of this example, thermal resistance can miss efficiently the heat generated with the rear face of LSI11 to the package exterior through the small pattern 32 for thermolysis, and the solder ball 33 for thermolysis.

[0033] 5th example drawing 5 is drawing showing the composition of MBGA which constitutes the 5th example of this invention, (a) shows the rear-face perspective diagram and (b) shows the fragmentary sectional view, respectively. Although the fundamental structure of MBGA of this example is the same as the 1st example, it differs in the following points. The metal base is divided into the grand pattern 37 of the shape of a ring of the package periphery section, the pattern 36 for power supplies of the center which separated predetermined distance from this grand pattern 37, and has been arranged, and the land pattern 29 of a large number arranged in the grand ring-like pattern 37. Thus, it is possible to form the grand pattern 29 for signals insulated from now on in the grand pattern 37. The chip capacitor 35 is attached in the gap of the grand pattern 37 of the shape of a ring of a ground potential, and the pattern 36 for power supplies of power supply potential with high-melting point solder. the portion of each exposed metal base -- solder ball 19B for GND is formed in the grand pattern 37, and solder ball 19C for power supplies is formed in the pattern 36 for power supplies for solder ball 19A for signals at the land pattern 29, respectively

[0034] it is also possible by boiling and changing various configurations of the metal base of the internal circuit pattern 17, the land pattern 29 and the pattern 36 for power supplies, and grand pattern 37 grade in the above-mentioned example to carry other chips other than a chip capacitor, for example, a chip resistor, a chip inductor, etc.

[0035] 6th example drawing 6 is the cross section showing MBGA of the 6th example of this invention. The package of this example is a package dealing with flip chip bonding which connected connection between the internal wiring 17 and the electrode of LSI11 by the minute flip chip bump 40. beforehand -- the internal wiring 17 top -- or an LSI11 top -- the flip chip bump 40 -- forming -- the internal wiring 17 and the electrode of LSI11 -- the flip chip bump 40 -- minding -- being the so-called -- flip chip bonding is carried out This flip chip bump 40 flows to the grand pattern 14 of the metal base through a through hole 22, and raises the thermolysis effect. The metal cap 28 pastes the polyimide layer 13 through the insulating adhesives 23, and closes LSI11 and internal wiring 17 grade airtightly in the building envelope. The upper surface and the metal cap 28 of LSI11 paste up with the thermally conductive adhesives 38. A generated heat part in LSI11 radiates heat easily through the metal cap 28 by the heat electroconductive glue 38. Furthermore, in order to plan the cooling effect, as shown in drawing 7 , a heat sink 39 is formed in the metal cap 28.

[0036] 7th example drawing 8 is drawing showing the structure of MBGA of the 7th example of this invention, and drawing (a) - (c) is the same drawing as drawing 1 (a) - (c). this example is the structure which made two-layer the copper foil pattern by the side of the metal base front face which constitutes the internal wiring 17. A through hole 22 performs the 1st layer and 2nd-layer electric flow between copper foil patterns. Numbers arbitrary [ two or more ] are possible for the number of layers of internal wiring. this example is an example which can respond to especially many pin-ization easily.
[0037] Octavus example drawing 9 is drawing for the octavus example of this invention being shown, and this drawing (a) - (g) corresponds to sequential process (a) - (g), and shows the fundamental manufacture method of the MBGA package concerning this invention with the cross section of this MBGA.
[0038] A metal laminated circuit board is formed by forming the polyimide layer 42 of 0.20 - 0.55-micrometer **, and forming the copper foil 43 of 0.18 - 0.35-micrometer ** on it further on a process (a) 0.15 - the 0.20mm metal base 41 which is the metal plate of **. The following processes are carried out by being made from this metal laminated circuit board.
[0039] The metal base 41 is formed in the grand pattern 14 and the land pattern 18 by patterning using the process (b) photoresist.
[0040] The whole region including the rear face of the metal base patterns 14 and 18 is coated with the masking resin 46 after (Process c) resist ablation. Subsequently, patterning of the copper foil 43 by the side of a front face is carried out, and the copper foil opening 45 for through holes is formed. Opening for a cavity is also formed in copper foil 41 if needed.
[0041] The polyimide layer 42 is **********ed by using process (d) copper foil 43 as a mask, and the polyimide opening 47 to which a metal base pattern is exposed is formed. In this case, it is also possible to form the cavity section shown in the example 2.
[0042] Nickel plating 48 is performed by no electrolyzing all over (Process e) front-face side, and the surface portion of a through hole 22 is formed. Thereby, the copper foil pattern 41 by the side of a front face and the metal base patterns 14 and 18 by the side of a rear face flow electrically through a through hole 22. Furthermore, by electrolysis plating which uses as an electrode the through hole portion which carried out electroless deposition, nickel plating is performed and nickel is further embedded in a through hole 22. Here, other metals, such as not only nickel but copper or a tungsten, are sufficient as each of electroless deposition and electrolysis plating.
[0043] The internal wiring 17 is formed by carrying out regist patterning of the copper foil 41 on the front face of a process (f) to a desired pattern.
[0044] Process (g)
The coating material 46 on the back is removed, and non-electrolyzed nickel plating and gold plate are performed to the pattern of the both sides by the side of a front face and a rear face. Thereby, MBGA of the example of this invention is obtained. In addition, washing and heat treatment are performed if needed between each process.
[0045] 9th example drawing 10 is process drawing showing the 9th example of this invention, and shows the manufacture method of the BGA package of one example of this invention one by one. As shown in this drawing, the 1st substrate 50 is formed by process (a) - (d), the 2nd substrate 55 is formed by process (a') - (g'), bonding of each of both substrates is carried out by process [ of the next step ] (h) - (j), and they is formed in one BONDEDDO substrate 56. Especially this example method is suitable for manufacturing the package dealing with flip chip bonding. In addition, washing and heat treatment are suitably performed between each process.
[0046] The polyimide layer 42 of 0.20 - 0.55-micrometer ** is formed on a process (a) and the 0.15 (a') - 0.20mm metal base 41 of **, and subsequently, the copper foil 43 of 0.18 - 0.35-micrometer ** is formed, and it considers as a metal laminated circuit board. In addition, the quality of the material and thickness are corrected suitably if needed.
[0047] Patterning of a process (b) and the copper foil (b') 43 is carried out, and the opening 45 for through holes is formed in a predetermined position.
[0048] Patterning of the polyimide layer 42 is carried out by using a process (c) and the copper foil (c') pattern 43 as a mask, the polyimide opening 47 for through holes is formed, and the metal base 41 is exposed in the portion.
[0049] The polyimide opening 47 is embedded by nickel plating 49 by electrolysis plating which uses a process (d) and the metal (d') base 41 as an electrode. This forms a through hole and electrical installation of the metal base 41 and copper foil 43 is performed. Here, it plates so that the several micrometers - about dozens of micrometers nickel plating 49 may project from the front face of the polyimide layer 42. Let a process (d) and (d') the substrate formed, respectively be the 1st metal wiring substrate 50 and the 2nd metal substrate 51.
[0050] All over the front-face side of the metal substrate 51 of a process (e') 2nd, spin coating of the polyimide layer 52 is carried out further.
[0051] Regist patterning is performed to the polyimide layer 52 of the metal wiring substrate 51 of a process (f') 2nd, and the opening 53 for through holes is formed so that it may come to the predetermined position on the copper foil pattern 43. Here, opening 53 exposes the copper foil pattern 43.
[0052] Process (g')
By electrolysis nickel plating which uses the copper foil pattern 43 of the 2nd metal wiring substrate 51 as an electrode, nickel 54 is embedded at opening of the polyimide layer 53, and the through hole electrically connected with the copper foil pattern 43 is formed. This obtains the 2nd metal wiring substrate 55. Here, from the front face of the polyimide layer 52, nickel plating 54 forms so that several micrometers - about dozens of micrometers may project.
[0053] Process (h) It goes and each front-face side of the 1st metal wiring substrate 50 and the 2nd metal wiring substrate 55

is made into doubling, and it aligns so that each copper foil pattern 43 and the plated metals 49 and 54 which the other party projected may touch in a desired position. Moreover, it is also possible to align so that each plating lobes 49 and 54 may face each other partly like illustration in this case.

[0054] Process (i) The 1st metal wiring substrate 50 and the 2nd metal wiring substrate 55 are made to rival with a thermocompression bonding press. Otherwise, adhesion using adhesives or the chemical reaction is sufficient as this cladding. Thereby, the BONDEDDO substrate 56 by which the metal base 41 was formed in the front face and the rear face is formed.

[0055] Patterning of the metal base 41 exposed to the field of the both sides of (Process j) BONDEDDO substrate 56 is carried out, respectively. In this case, the metal base 41 of the 1st metal wiring substrate 50 is formed in the ring pattern 30 and the flip chip bump 40, and the metal base of the 2nd metal wiring substrate 51 performs patterning, where a front face is coated, and it forms it in the usual grand pattern 14 and the usual land pattern 18. After carrying LSI in the 1st metal wiring substrate 50 side by flip chip bonding, an airtight is acquired by pasting up a cap on the ring pattern 30. It has flowed through the flip chip bump 40 and the ring pattern 30, the land pattern 18, and the grand turn 14 mutually electrically through the copper foil pattern 43 and through holes 49 and 54.

[0056] 10th example drawing 11 is drawing showing the structure of the semiconductor device containing MBGA of the 10th example of this invention, and it is the plan in which drawing (a) shows the cross section after packaging, and (b) shows the interior. The structure of this example adopts the manufacture method of for example, the 9th example, and is formed. In addition, although this example is explained as a multi chip package, it is applicable also to a single chip package.

[0057] The height of the flip chip bump 40 and the electrode 62 for chips which were obtained by carrying out patterning of the metal base by the side of a front face, and the ring pattern 30 is 50-100 micrometers. The area of LSI59, the area of the chip of chip-capacitor 61 grade, or the area where LSI and a chip are intermingled is divided by the ring pattern 30, respectively. For example, when LSI of low frequency and LSI of a RF are assembled in the same package, as shown in drawing 11 , the cross talk between these LSI is reduced by closing each area by the metal cap 60, conductive resin 26, and the ring pattern 30. That is, electrostatic **** magnetic shielding becomes possible among two or more chips and between the exteriors with one package. LSI59 is connected with the flip chip bump 40 using adhesives or a low melting point metal. An LSI rear face is pasted up with the metal cap 60 through the high temperature conduction resin 38. The height of the land pattern 18 obtained by carrying out patterning of the metal base by the side of a rear face and the grand pattern 14 is 150-200 micrometers.

[0058] With the MBGA package which used the metal substrate of each above-mentioned example for material, the following effect and advantages arise by using a metal with high thermal conductivity, for example, copper, for a base substrate, forming each pattern and a through hole with regist-patterning technology, and performing a hermetic seal with a cap.

[0059] By using the metal of high temperature conductivity for the base substrate of a package, thermal resistance is small and thermolysis nature improves. In forming especially a cavity and carrying LSI in the metal base directly, thermolysis nature improves much more.

[0060] Moreover, with the package of each above-mentioned example, since a through hole is formed by the photoresist and etching, formation of the detailed through hole of 20-30 micrometerphi is attained. For this reason, in case plating is embedded in a through hole, the interior of a through hole is completely filled by the plated metal. Therefore, unlike the conventional BGA, there is no fear of an invasion of the moisture from a through hole. Furthermore, if a metal cap is employed, especially, good hermetic-seal structure will become possible and there will be no fear of an invasion of the moisture from a cap and its circumference. Moisture resistance of MBGA improves for the above reason.

[0061] In addition, since there is a possibility that moisture may invade from a polyimide layer in adopting the structure which the polyimide layer of an insulator exposes, it is desirable to avoid the invasion of moisture using the metal laminated circuit board which coated the polyimide layer front face with the fluorine system resin, or replaced the polyimide layer, other insulators, for example, Teflon layer.

[0062] Next, the connection resilience and reliability at the time of mounting of MBGA of this invention are considered. With the conventional mounting structure, the coefficient of thermal expansion of a printed circuit board and the coefficient of thermal expansion of a package are made almost equal. However, depending on the size and the helicopter loading site of a printed circuit board, it is hard to avoid, stress occurs on a solder ball, and the difference of an expansion coefficient becomes the factor as which it determines the reliability and the life of a semiconductor device which were mounted in fact. In MBGA of the above-mentioned example, to the coefficient of thermal expansion of a printed circuit board, since the coefficient of thermal expansion of a polyimide layer is large, thermal stress occurs between these material. Moreover, the stress generated by substrate size and the helicopter loading site is also added to this. However, the solder ball is formed on the 0.15-0.20-micrometer pillar-like metal base (land pattern), when the metal base of the shape of this pillar moves focusing on an adhesion interface with a polyimide layer, the thermal stress generated on the solder ball is absorbed with the metal base of the shape of this pillar, and the reliability and the life at the time of mounting are prolonged as compared with the conventional package.

[0063] Considering an electrical property side, in MBGA of this invention, it is easy to form internal wiring in microstrip-line structure. Moreover, by optimizing the path of a land pattern and a grand pattern, it can form so that it may have coaxial structure with a desired characteristic impedance. Furthermore, as shown, for example in the 10th example, chips, such as a chip capacitor, can be carried by choosing the pattern of the metal base suitably. Furthermore, the cross talk noise between wires is also reduced by adoption of hermetic-seal structure. By these, it becomes easy to take adjustment of an impedance

inside a package. moreover, by pasting up a metal cap and the metal base by conductive resin, and making both potentials into grounding potential, from the outside, the inside of a package is boiled electrically and magnetically, and is shielded By adopting this composition, use of LSI is attained also in a RF field.
[0064] In addition, the material which constitutes a metal substrate can be selected suitably. For example, the metal base can consider the other various metal of the metal which makes copper or aluminum a principal component.
[0065]
[Effect of the Invention] As mentioned above, with the package for semiconductor devices of this invention, as explained, while the semiconductor chip could be closed by the high airtight structure and the performance of a semiconductor device could maintain highly by composition which adopted the metal base, when it applies to the semiconductor device for RFs, a microstrip line, etc., a semiconductor device with the high performance which responds to the performance required of these can be manufactured.

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[Translation done.]

## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] For a front flat-tapped section notch perspective diagram and (b), in drawing showing the structure of the 1st example of this invention, a rear-face perspective diagram and (c) are [ (a) ] a fragmentary sectional view.
[Drawing 2] For a front flat-tapped section notch perspective diagram and (b), in drawing showing the structure of the 2nd example of this invention, a rear-face perspective diagram and (c) are [ (a) ] a fragmentary sectional view.
[Drawing 3] In drawing showing the structure of the 3rd example of this invention, (a) is a fragmentary sectional view and (b) is a rear-face perspective diagram.
[Drawing 4] In drawing showing the structure of the 4th example of this invention, (a) is a fragmentary sectional view and (b) is a rear-face perspective diagram.
[Drawing 5] In drawing showing the structure of the 5th example of this invention, (a) is a rear-face perspective diagram and (b) is a fragmentary sectional view.
[Drawing 6] The fragmentary sectional view showing the structure of the 6th example of this invention.
[Drawing 7] The fragmentary sectional view showing the structure of the 6th example of this invention.
[Drawing 8] For a front flat-tapped section notch perspective diagram and (b), in drawing showing the structure of the 7th example of this invention, a rear-face perspective diagram and (c) are [ (a) ] a fragmentary sectional view.
[Drawing 9] The cross section showing the manufacturing process of the octavus example of this invention one by one.
[Drawing 10] The cross section showing the manufacturing process of the 9th example of this invention one by one.
[Drawing 11] In drawing showing the structure of the 10th example of this invention, (a) is a cross section and (b) is a plan.
[Drawing 12] drawing showing the 1st conventional technology -- (a) -- a front flat-tapped section notch perspective diagram and (b) -- a rear-face perspective diagram and (c) -- a fragmentary sectional view
[Drawing 13] drawing showing the 2nd conventional technology -- (a) -- a front flat-tapped section notch perspective diagram and (b) -- a rear-face perspective diagram and (c) -- a fragmentary sectional view
[Drawing 14] drawing showing the modification of the 2nd conventional technology -- (a) -- a front flat-tapped section notch perspective diagram and (b) -- a rear-face perspective diagram and (c) -- a fragmentary sectional view
[Drawing 15] The cross section showing the 3rd conventional technology.
[Description of Notations]
11 LSI
12 Cap
13 Polyimide
14 Grand Pattern
15 Island Pattern
17 Internal Circuit Pattern
18 Land Pattern
19 Solder Ball
20 Adhesives
21 Bonding Wire
22 Through Hole
23 Insulating Adhesives
24 Cavity
25 Coating
26 Electroconductive Glue
27 Coating Resin
28 Metal Cap
29 Grand Pattern
30 Ring Pattern
32 Thermolysis Pattern
33 Solder Ball for Thermolysis
34 Solder Resist

35 Chip Capacitor
36 Power Supply Pattern
37 Grand Pattern
38 Heat Electroconductive Glue
39 Heat Sink
40 Flip Chip Bump
41 Metal Base
42 Polyimide
43 Copper Foil
44 Resist Pattern Opening
45 Copper Foil Opening
46 Masking Resin
47 Polyimide Opening
48 Metal Plating
49 Copper Foil Patterning Section
50 Through Hole
51 Nickel Plating
52 Copper Foil Pattern
59 LSI
60 Metal Cap
61 Chip Capacitor
62 Electrode for Chips
101 LSI
102 Closure Resin
103 Internal Wiring
104 Through Hole
105 Solder Resist
106 Glass Epoxy-Group Board
108 Solder Ball
109 Solder Ball for Thermolysis
110 Through Hole for Thermolysis
111 External Wiring
112 Bonding Wire
113 Plastics Mould
114 Island Pattern
115 Ag Paste
116 Through Hole for Thermolysis
116 ** Solder Ball for Thermolysis 116 117
118 Substrate 118
119 Beer Hall
120 LSI
121 TAB Lead
122 Wiring
123 Signboard
124 Solder Ball
125 Bump

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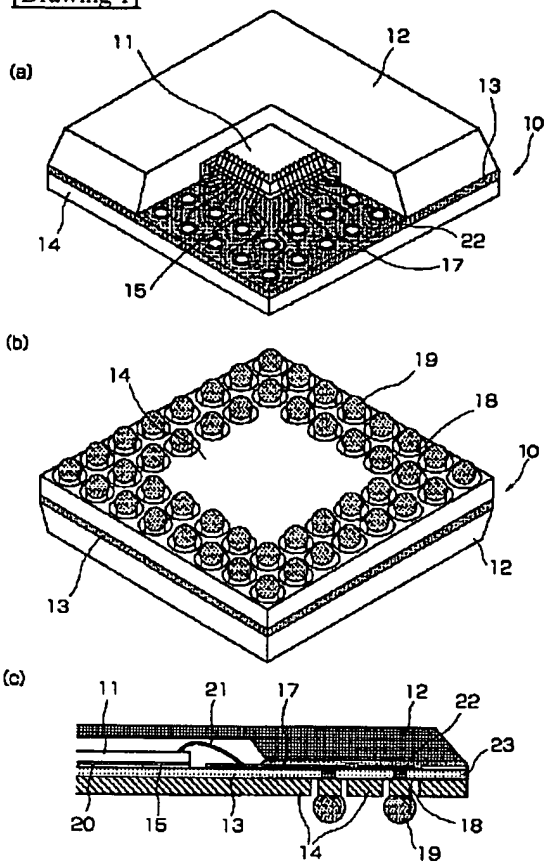
[Translation done.]

* NOTICES *

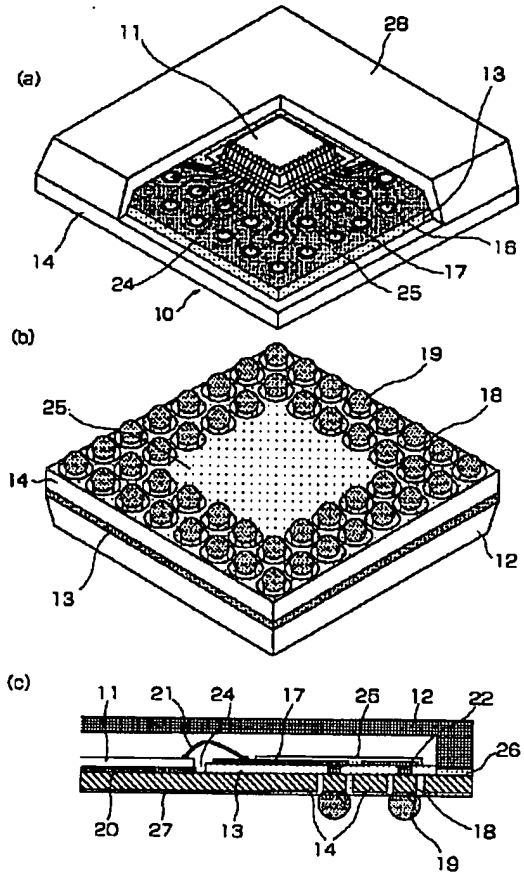


DRAWINGS

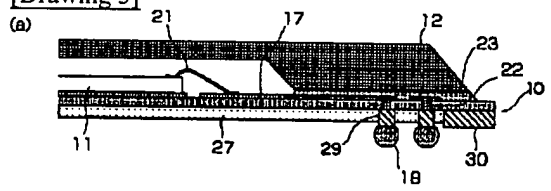
[Drawing 1]

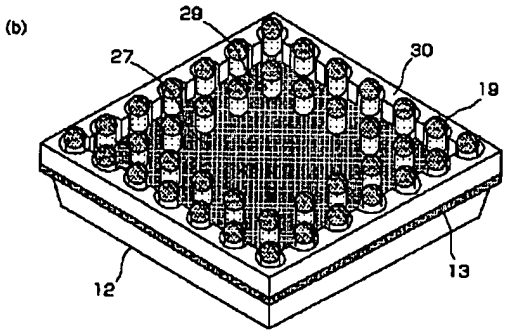



[Drawing 2]



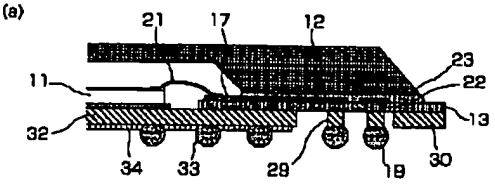

[Drawing 3]



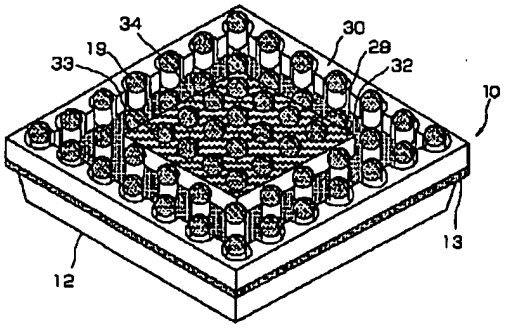




[Drawing 4]

(a)

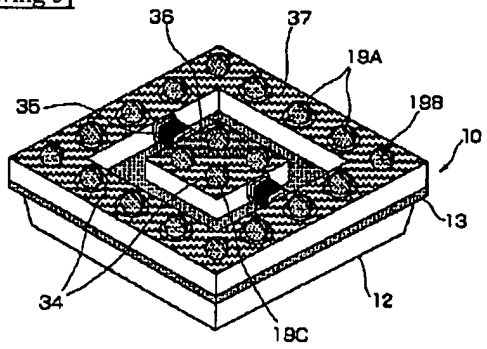



(b)

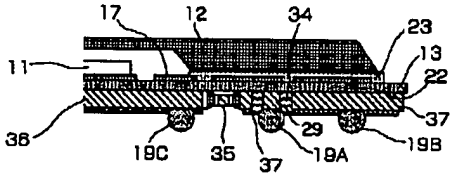



[Drawing 5]

(a)




(b)

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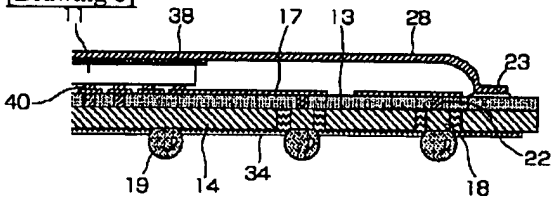


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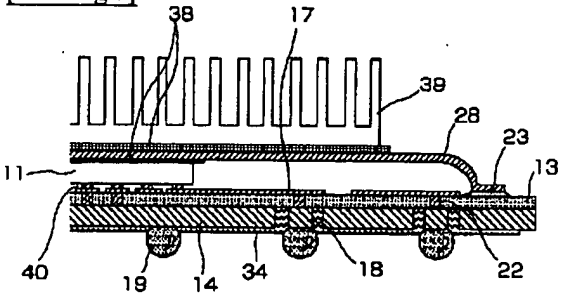

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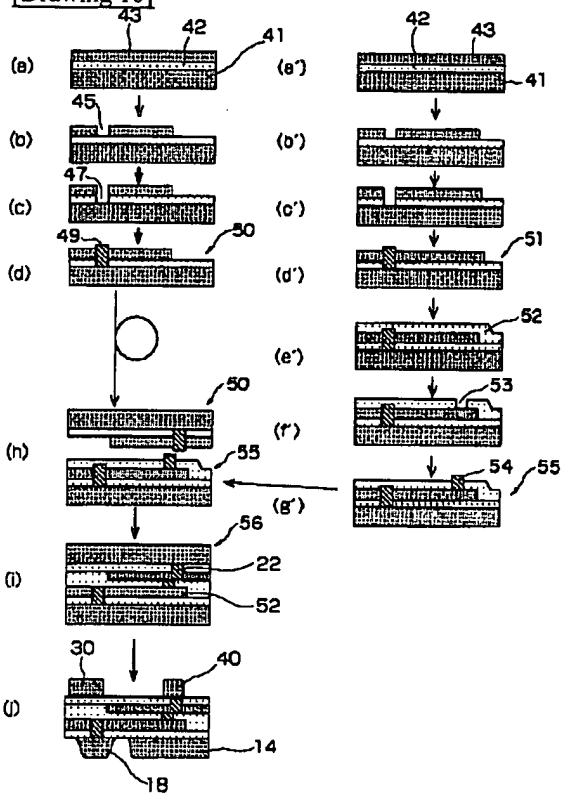


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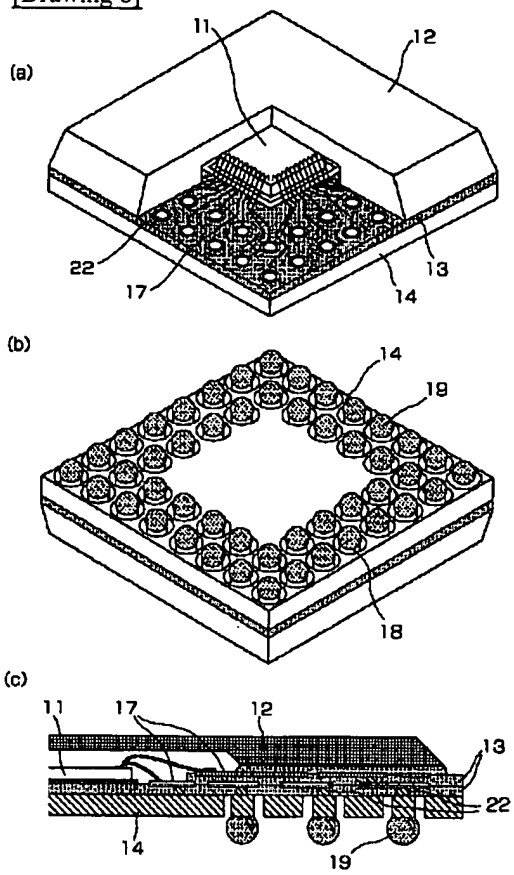
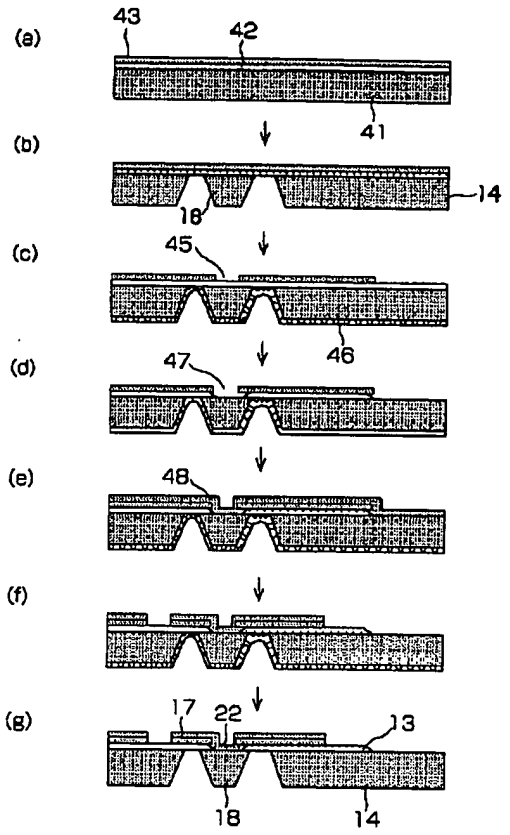
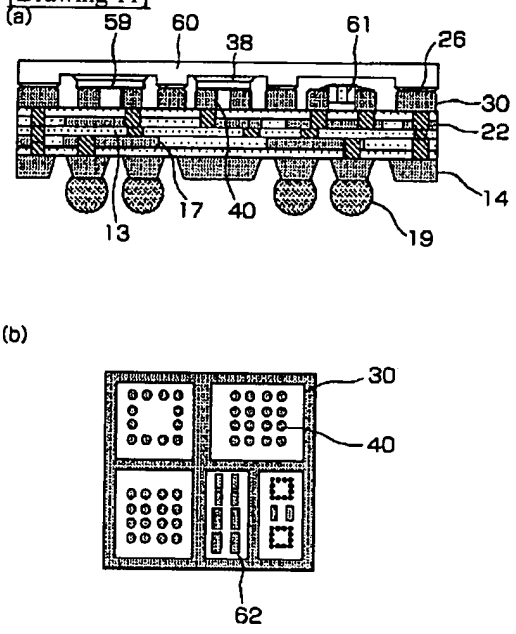



[Drawing 9]




[Drawing 11]

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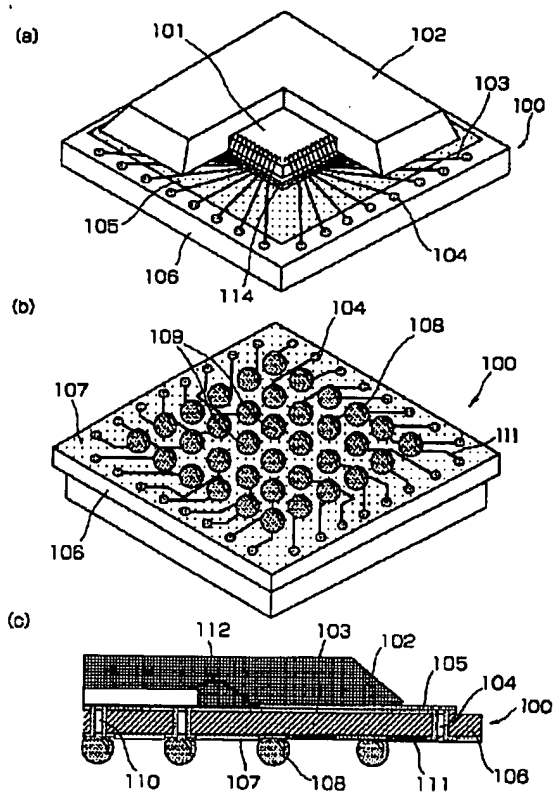


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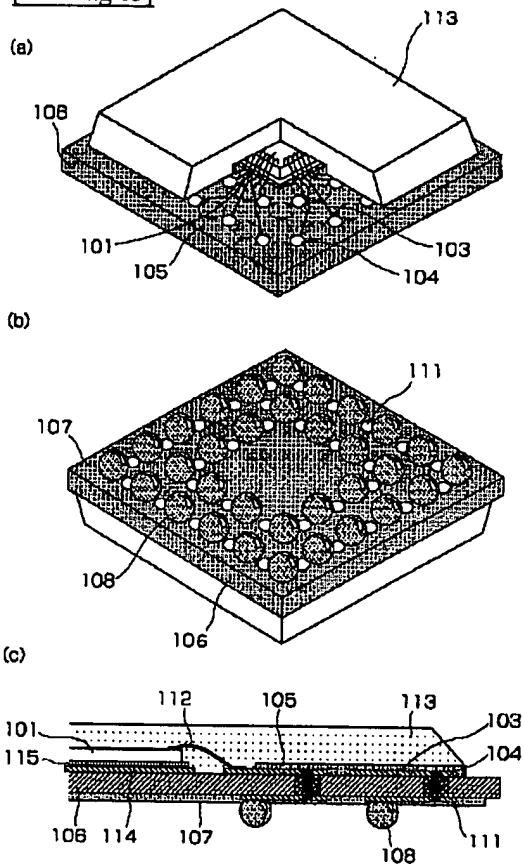


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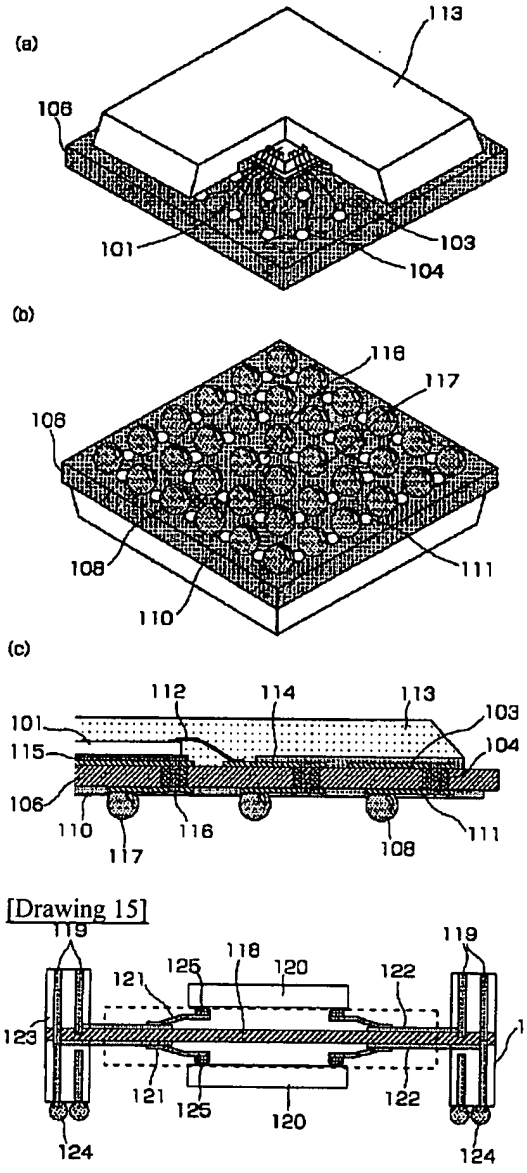


[Drawing 15]




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[Translation done.]